4-A Peak, High Voltage, High Frequency High-Side and Low-Side Driver

1. Description

The MD18211A high-frequency gate driver includes a 120-V bootstrap diode, and is designed to drive both high-side and low-side N-Channel MOSFETs with maximum control flexibility of independent inputs.

The inputs can handle -10V to 20V DC, which increases robustness against ringing from gate transformers and/or parasitic inductance of long routing traces.

High side driver is designed to be protected from negative spikes at HS pin as low as -18V, caused by parasitic inductance and stray capacitance.

15ns rising and 14ns falling propagation delay allows the systems operating at high frequency with less delay matching variations.

The MD18211A is offered in DFN 4X4-8 pins, DFN 4X4-10 pins, ESOP-8 package.

MD18211ATDAC: The net weight of a single capsule is 42.74mg.

2. Typical Applications

- Power Supplies for Telecom, Datacom, and 48V to 72V Battery Powered Systems
- Half-Bridge Applications and Full-Bridge Converters
- Push-Pull Converters
- High Voltage Synchronous Buck Converters
- Two-Switch Forward Converters
- Active Clamp Forward Converters
- Class-D Audio Amplifiers

3. Features

- Drives Both High-Side and Low Side N-Channel MOSFETs with Independent Inputs
- Operating Switching Frequency up to 1MHz
- Bootstrap Supply Voltage up to 120V DC
- 4-A Source and Sink Output Peak Currents
- 5-ns Rise and 4-ns Fall Time with 1000-pF Load
- Input Pins Can Tolerate -10V to +20V, and are Independent of Supply Voltage Range
- TTL Compatible Inputs
- 8V to 17V VDD Operating Range, 20V ABS MAX
- Fast Propagation Delay Times
- Excellent Propagation Delay Matching (1ns Typical)
- Symmetrical Undervoltage Lockout for High-Side and Low-Side Driver
- Available in DFN 4X4-8, DFN 4X4-10, ESOP-8 package
- Specified from -40°C to 140°C

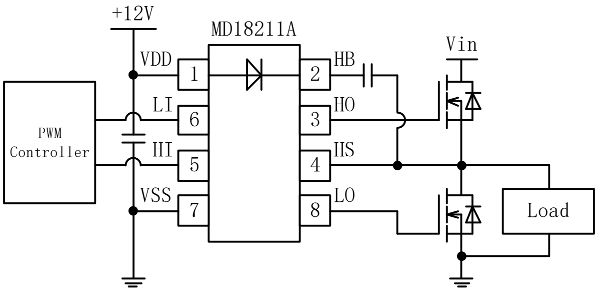
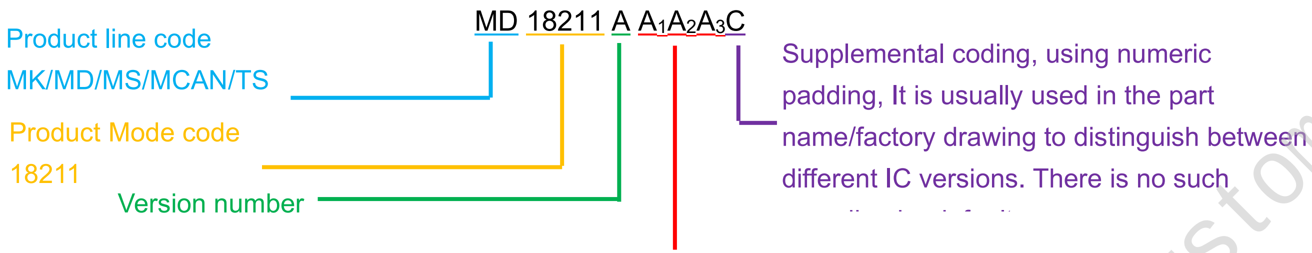


Figure 1. Typical Application Diagram

4. Order Information



Supplemental coding, using numeric padding, It is usually used in the part name/factory drawing to distinguish between different IC versions. There is no such

Encapsulation encoding

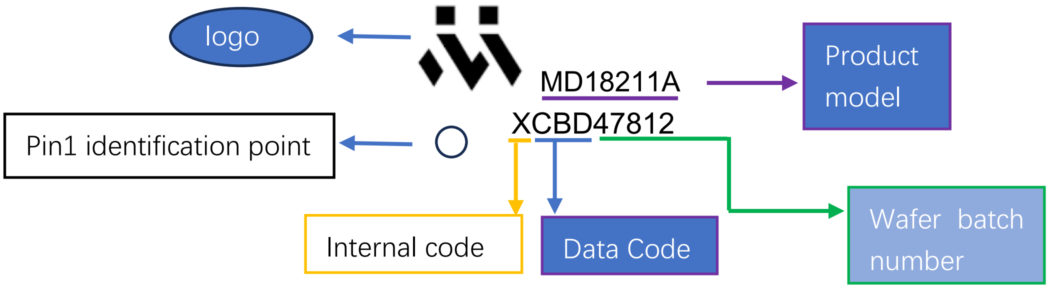
A2A3: Encapsulated form code;

A1: 1. For products containing MOS or GAN encapsulation, the model representing MOS or GAN;

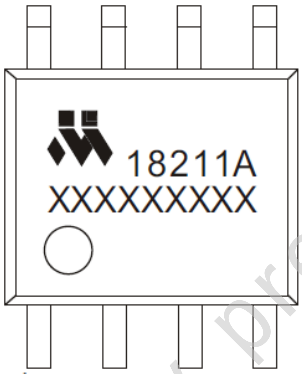
2. For products that do not contain MOS or GAN, in principle, the letter "X" is uniformly used; In special cases, it can be used as the identification of special specifications of products, using A/B/C... and other letters instead;

Order Code	Package	Pins	SPQ (pcs)
MD18211ATDAC	DFN 4X4	8	5000
MD18211ATDD	DFN 4X4	10	5000
MD18211ATAD	ESOP	8	4000

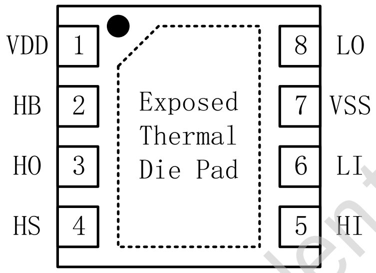
5. Package Reference and Pin Functions



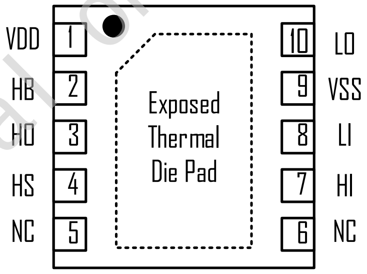
(please refer to MRX-DM-SCM-04 for detailed rules)



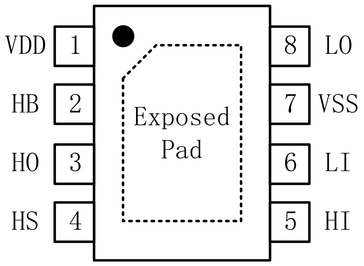
MD18211A top marking data code



DFN-8 4X4 (top view)



DFN-10 4X4 (top view)



ESOP-8 (top view)

Pin Number	Name	Description
1	VDD	Positive gate drive supply. Locally decouple to VSS using low ESR/ESL capacitor located as close to the device as possible
2	HB	High-side bootstrap supply. Connect to the positive terminal of bootstrap capacitor that should be placed as close to the device as possible.
3	HO	High-side gate driver output. Connect to the gate of high-side MOSFET with a short, low inductance path
4	HS	High-side source connection. Connect to the negative terminal of bootstrap capacitor and the source of the high-side N-Channel MOSFET
5	HI	High-side input
6	LI	Low-side input
7	VSS	Negative supply for the device that is generally grounded. All signals of the device are referenced to this ground
8	LO	Low-side gate driver output. Connect to the gate of low-side MOSFET with a short, low inductance path

6. Specifications

6.1 Absolute Maximum Ratings (1)

VDD, HB-HS	–0.3V to +20V
LI, HI	–10V to +20V
HS-VSS DC	–5V to +110V
Repetitive pulse (2)	–18V to +115V
LO DC	–0.3V to VDD+0.3V
Repetitive pulse (2)	–2V to VDD+0.3V
Repetitive pulse (3)	–5V to VDD+0.3V
HO-HS DC	–0.3V to VDD+0.3V
Repetitive pulse (2)	–2V to VDD+0.3V
Repetitive pulse (3)	–5V to VDD+0.3V
HB-VSS	–0.3V to +120V
Power Dissipation at TA = +25°C (4)	2.7W
Junction Temperature	-40°C to 150°C
Lead Temperature (Solder)	260°C
Storage Temperature	–65°C to +150°C

6.2 Recommend Operation Conditions (5)

VDD	8V to 17V
HS-VSS DC	-1V to 105V
Repetitive pulse (2)	–15V to +110V
HB-VSS	HS+8V to HS+17V
	VDD-1V to 115V
HS Slew Rate	<50V/ns
Maximum Junction Temp. (T_J)	-40°C to +140°C
Ambient Temperature	-40°C to 125°C

6.3 Thermal Resistance (6)

	θ_{JA}	$\theta_{JC(TOP)}$	$\theta_{JC(BOT)}$
4X4 DFN-8	37.8	47.4	4.6°C/W
4X4 DFN-10	40	48.8	4.8°C/W
ESOP-8	30.2	42.3	5.8°C/W

Notes:

(1) Exceeding these ratings may cause permanent damage to the device

(2) Repetitive pulse ≤100ns. Verified at bench characterization

(3) Repetitive pulse ≤30ns. Verified at bench characterization

(4) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature.

(5) The device is not guaranteed to function outside of its operating conditions.

(6) Measured on JEDEC, 1S0P PCB.

6.4 ESD Ratings

		Value	Units
Electrostatic discharge V$_{ESD}$	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±2000	V

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.5 Recommended reflow profile

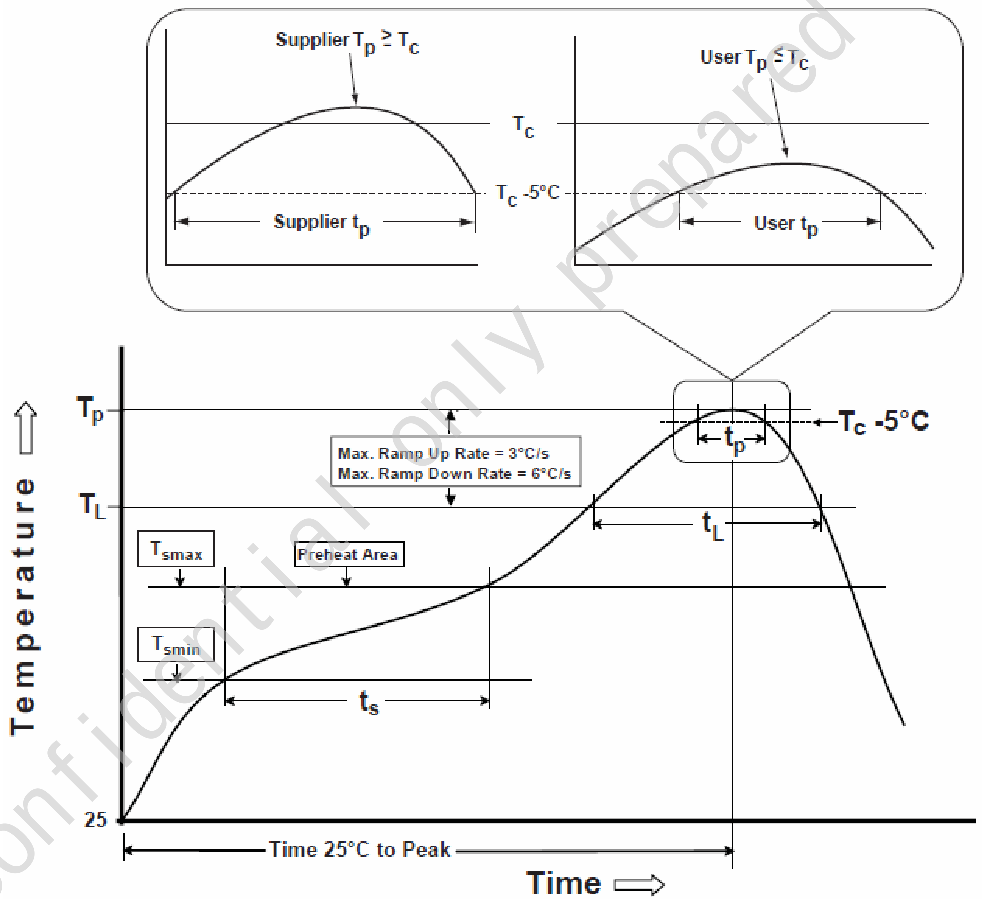


Figure 2. reflow curve

Table1. SnPb Eutectic Process-Classification Temperatures (TC)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 ℃	220 ℃
⩾2.5 mm	220 ℃	220 ℃

Table2. Pb-Free Process-Classification Temperatures (TC)

Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ >2000
<1.6 mm	260℃	260℃	260℃
1.6 mm-2.5 mm	260℃	250℃	245℃
>2.5 mm	250℃	245℃	245℃

Table3. Classification reflow profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	100 ℃ 150℃ 60-120 seconds	150 ℃ 200 ℃ 60-120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature (T_L) Time (t_L)maintained above T_L	183℃ 60-150 seconds	217℃ 60-150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the classification temp in Table1 For suppliers T_P must equal or exceed the classification temp in Table1	For users T_P must not exceed the classification temp in Table2 For suppliers T_P must equal or exceed the classification temp in Table2
Time (t_P) within 5℃ of the specified classification temperature (T_C)	20 seconds	30 seconds
Ramp-down rate (T_P to T_L) Time 25℃ to peak temperature	6℃/second max 6 minutes max	6℃/second max 8 minutes max
*Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum		

6.6 Recommended Wave Soldering Profile

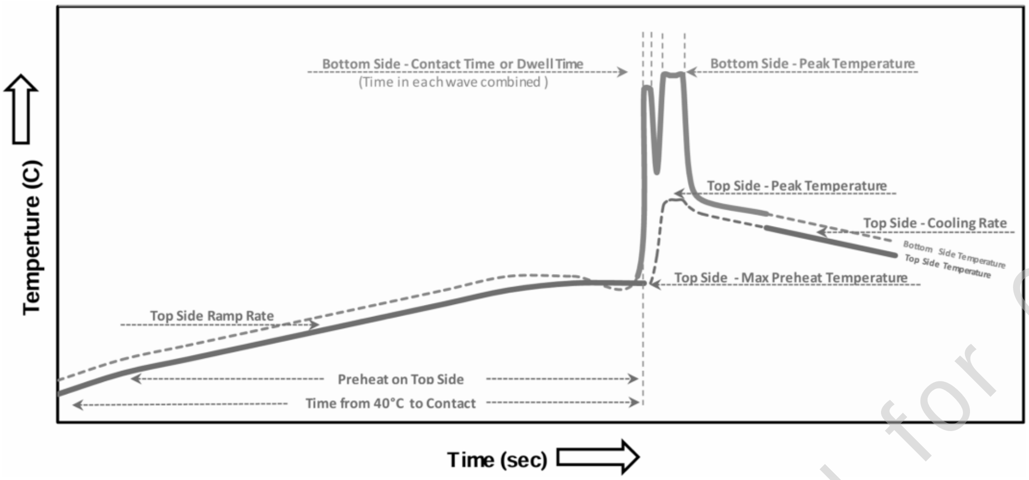


Figure 3. Wave Soldering Curve

Recommended Parameters for Solder Pot Temperature

Profile Feature	General Profile IPC/JEDEC [1]
Tin-Lead Alloys	230 – 260 °C
Lead-Free Alloys	260 – 290 °C

*Temperatures can start as low as 240°C depending on the application and alloy being used.

Recommended Parameters for VOC-Free

Profile Feature	General Profile IPC/JEDEC[1]	Tin-Lead Alloys (Recommended starting point) [2]	Lead-Free Alloys (Recommended starting point) [3]
Top Side Ramp Up Rate	< 3 °C/ Sec.	1 - 3 °C/ Sec.	1 - 3 °C/ Sec.
Top Side Max Preheat Temperature	< 150 °C	90 – 120 °C	90 – 140 °C
Bottom Side Contact Time	< 10 Sec.	< 5 Sec.	< 8 Sec.
Top Side Cooling Rate	< 3 °C / Sec.	< 3 °C / Sec.	< 3 °C / Sec.
Time from 40°C to Contact	60 – 240 Sec.	60 – 180 Sec.	60 – 180 Sec.

Notes:

(1) The general profile data are the parameters allowable by IPC/JEDEC, and are added only as a reference.

(2) This data guideline applies to common tin-lead alloys (i.e. Sn63/Pb37, Sn62/Pb36/Ag2).

(3) This data guideline applies to common lead-free alloys (i.e. AIM REL Alloys, SAC, SN100C et.al.).

6.7 Recommended Hand Soldering and Desoldering Methods

Hand Soldering

Selection of soldering iron	Flux	Iron temperature	Welding time
Sharp tip or cutting head	Use rosin type or non-cleaning flux (with a small amount of auxiliary wetting)	Sn Pb solder: 300-350℃ Lead free solder: 350-400 ° C	2-4 seconds per solder joint (to avoid overheating and damaging components or PCBs)

Notes:

(1) Heat the solder pad first, then send the solder wire.

(2) Avoid forcefully pressing the soldering iron tip.

(3) Pay attention to hand soldering ESD.

Hand Desoldering

Selection of desoldering tool	Use solder suction cups and soldering irons	Use hot air gun
Solder sucker and soldering iron or Hot air gun	Iron temperature: Sn Pb solder: 300-350℃; Lead free solder: 350-400 ° C; Operation: Quickly heat the solder joint and then tin suction	Temperature: 300-400℃ Airflow: medium to low (to avoid blowing small components off). Time:≤10 seconds/solder joint. Preheating plate: 150-180 ° C (bottom heating). Hot air nozzle: 250-300 ° C (top heating).

Notes:

(1) Clean the residual solder flux on the solder pads after desoldering.

(2) Multilayer boards should be carefully avoided to prevent Pad detachment.

6.8 Electrical Characteristics

VDD=V_{HB}=12V, V_{HS}=VSS=0V, T_A=T_J=-40°C to +140°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Currents						
VDD quiescent current	I_{VDD}	V(LI)=V(HI)=0V		0.2	0.4	mA
VDD operating current	I_{VDDO}	f=500kHz, C_{LOAD}=0		0.8	1.2	mA
HB total quiescent current	I_{HB}	V(LI)=V(HI)=0V		0.15	0.3	mA
HB total operating current	I_{HBO}	f=500kHz, C_{LOAD}=0		0.8	1.2	mA
HB to VSS quiescent current	I_{HBS}	V(HS)=V(HB)=105V		4	11	µA
HB to VSS operating current	I_{HBSO}	f=500kHz, C_{LOAD}=0		0.05		mA
Inputs						
Input voltage rising threshold	V_{ITH}			1.9	2.4	V
Input voltage falling threshold	V_{ITL}		0.8	1.5		V
Input voltage hysteresis	V_{ITHYS}			0.4		V
Input pulldown resistance	R_{IN}		100	230	350	kΩ
Undervoltage Lockout						
VDD rising threshold	V_{DDR}		6.4	7.1	7.8	V
VDD threshold hysteresis	V_{DDHYS}			0.49		V
HB rising threshold	V_{HB}		6.0	6.8	7.5	V
HB threshold hysteresis	V_{HBHYS}			0.76		V
Bootstrap Diode						
Low-current forward voltage	V_{FL}	$I_{VDD\text{-}HB}$=100µA		0.62	0.84	V
High-current forward voltage	V_{FH}	$I_{VDD\text{-}HB}$=100mA		0.88	1.1	V
Dynamic resistance, $\Delta V_F/\Delta I$	R_D	$I_{VDD\text{-}HB}$=100mA and 80mA		0.74	1.12	Ω
Lo Gate Driver						
Low-level output voltage	V_{LOL}	I_{LO}=100mA		0.08	0.2	V
High-level output voltage	V_{LOH}	I_{LO}=-100mA, V_{LOH}=VDD-LO		0.11	0.25	V
Peak pull-up current		V_{LO}=0V		4		A
Peak pull-down current		V_{LO}=12V		4		A
Ho Gate Driver						
Low-level output voltage	V_{HOL}	I_{HO}=100mA		0.08	0.2	V
High-level output voltage	V_{HOH}	I_{HO}=-100mA, V_{HOH}=HB-HO		0.11	0.25	V
Peak pull-up current		V_{HO}=0V		4		A
Peak pull-down current		V_{HO}=12V		4		A
Propagation Delays						
LO turn-on propagation delay	T_{DLR}	LI rising to LO rising		15	30	ns
HO turn-on propagation delay	T_{DHR}	HI rising to HO rising		15	30	ns
LO turn-off propagation delay	T_{DLF}	LI falling to LO falling		14	30	ns
HO turn-off propagation delay	T_{DHF}	HI falling to HO falling		14	30	ns
Delay Matching						
From HO OFF to LO ON	T_{MON}			1	6	ns

From LO OFF to HO ON	T_{MOFF}			1	6	ns
Output Rise and Fall Time						
LO, HO rise time		C_{LOAD}=1nF		5		ns
LO, HO fall time		C_{LOAD}=1nF		4		ns
LO, HO rise time		C_{LOAD}=100nF		0.27	0.5	us
LO, HO fall time		C_{LOAD}=100nF		0.23	0.5	us
Miscellaneous						
Minimum input pulse width that changes the output					10	ns
Bootstrap diode reverse recovery time		I_F=20mA, I_R=200mA		90		ns

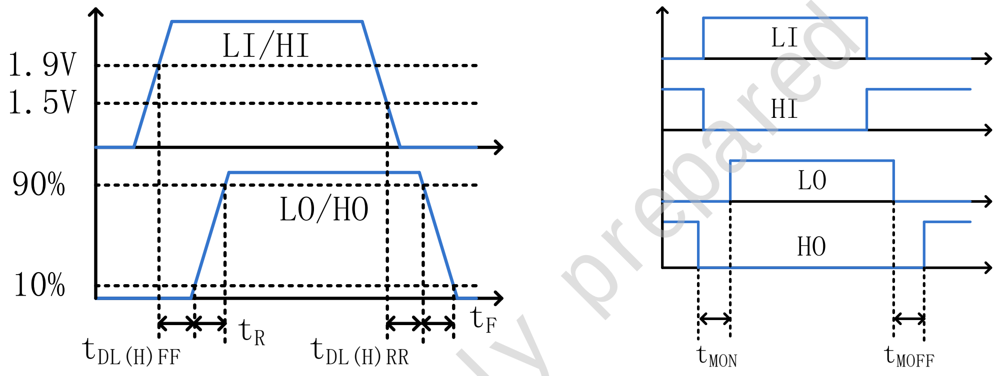


Figure 4. Timing Diagram

6.9 Typical Characteristics

Temp=25℃,VDD=HB=12V, C_{L_HO}= C_{L_LO}=0nF

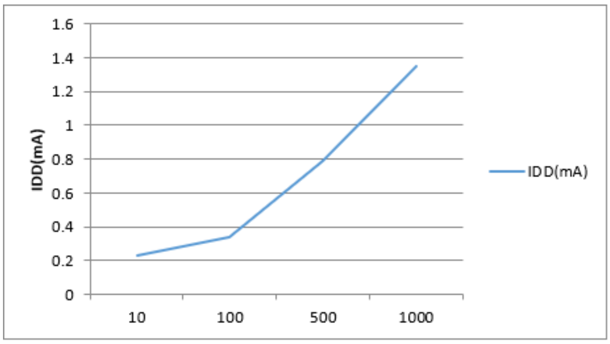


Figure 5. IDD Operating Current vs Frequency

Frequency=100kHz, VDD=HB=12V, C_{L_HO}= C_{L_LO}=0nF

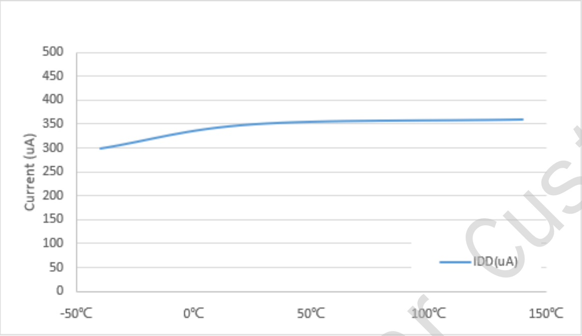


Figure 6. IDD Operating Current vs Temperature

Temp=25℃, VDD=HB=12V, C_{L_HO}= C_{L_LO}=0nF

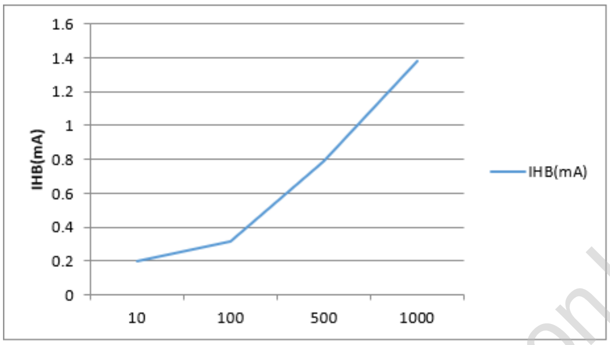


Figure 7. IHB Operating Current vs Frequency

Frequency=100kHz, VDD=HB=12V, C_{L_HO}= C_{L_LO}=0nF

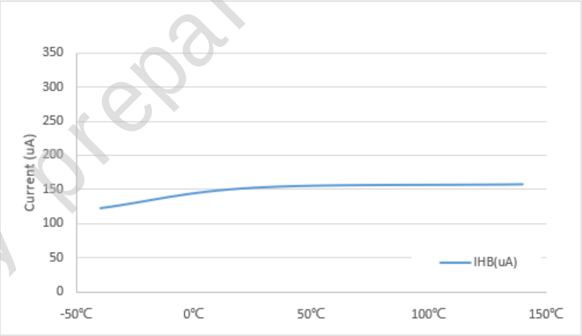


Figure 8. IHB Operating Current vs Temperature

Temp=25℃,C_{L_HO}= C_{L_LO}=0nF

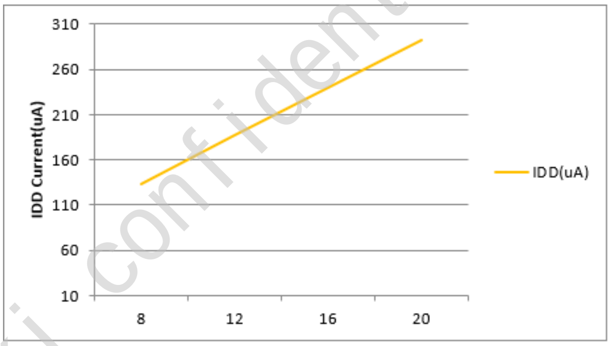


Figure 9. IDD Quiescent Current vs Supply Volt

VDD=12V,C_{L_HO}= C_{L_LO}=0nF

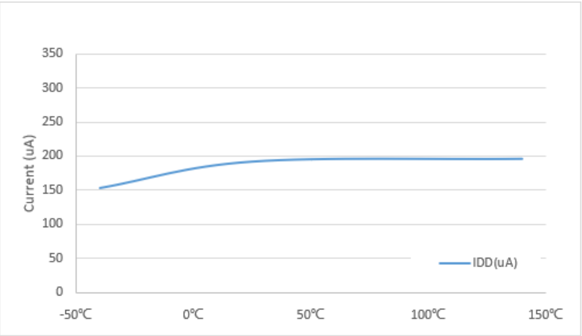


Figure 10. IDD Quiescent Current vs Temperature

Temp=25℃,C_{L_HO}= C_{L_LO}=0nF

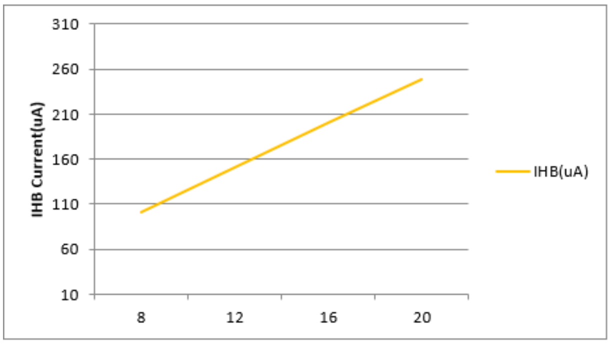


Figure 11. IHB Quiescent Current vs Supply Voltage

VHB=12V,C_{L_HO}= C_{L_LO}=0nF

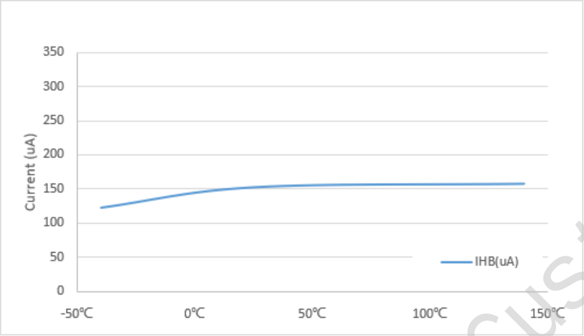


Figure 12. IHB Quiescent Current vs Temperature

Temp=25℃

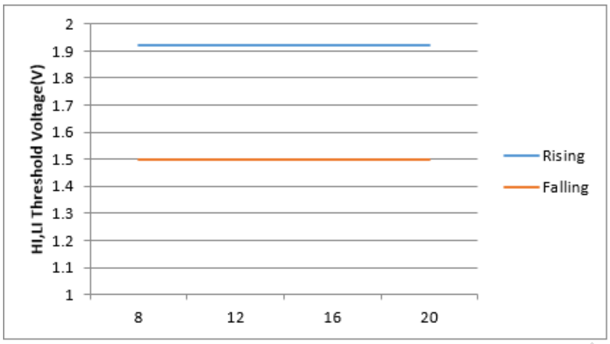


Figure 13. Input Threshold vs Supply Voltage

VDD=12V

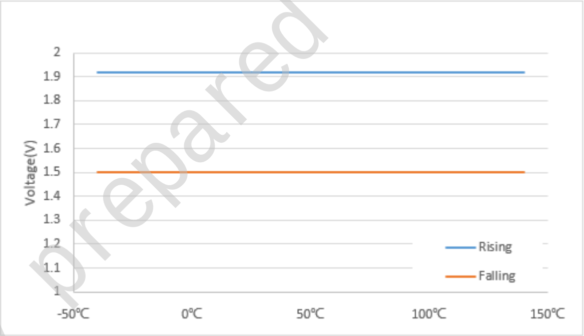


Figure 14. Input Threshold vs Temperature

VDD=12V

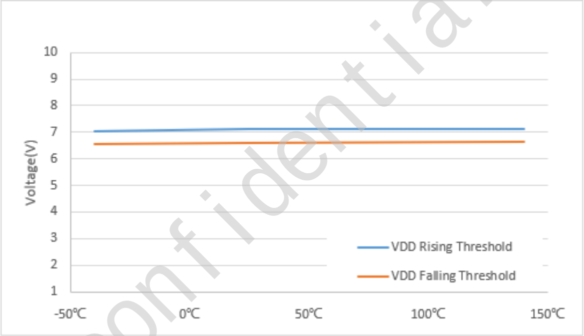


Figure 15. VDD threshold vs Temperature

VDD=12V

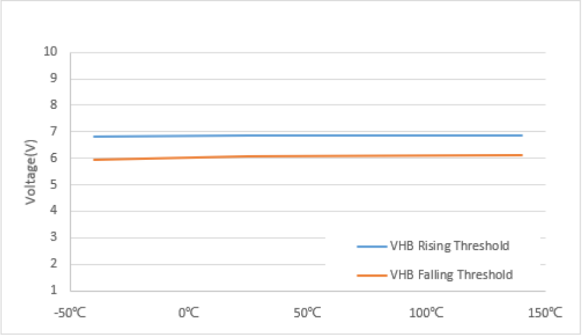


Figure 16. VHB threshold vs Temperature

VDD=12V

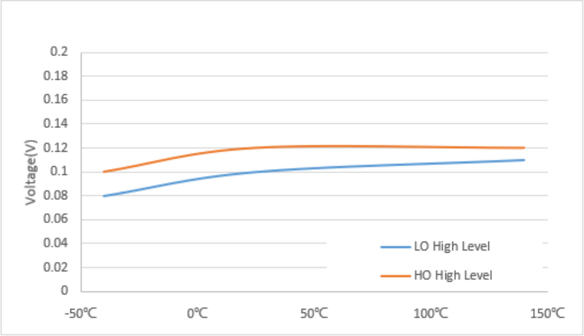


Figure 17. High Level Output Voltage vs Temperature

VDD=12V

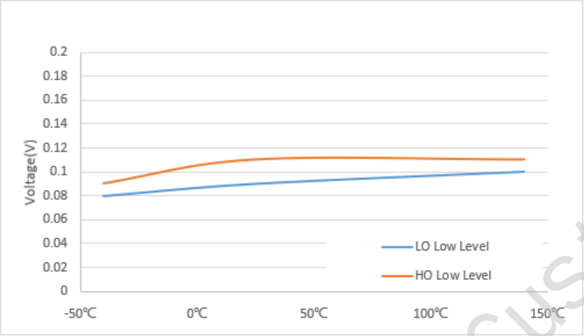


Figure 18. Low Level Output Voltage vs Temperature

VDD=12V,C_{L_HO}= C_{L_LO}=0nF

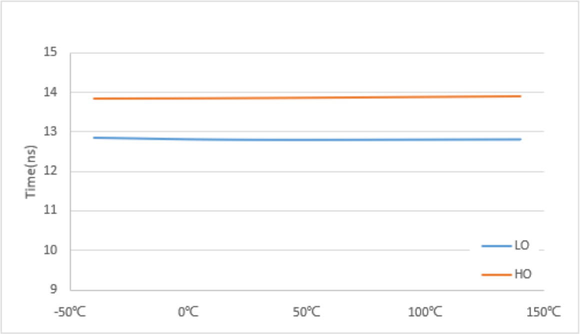


Figure 19. Turn Off Propagation Delay vs Temperature

VDD=12V,C_{L_HO}= C_{L_LO}=0nF

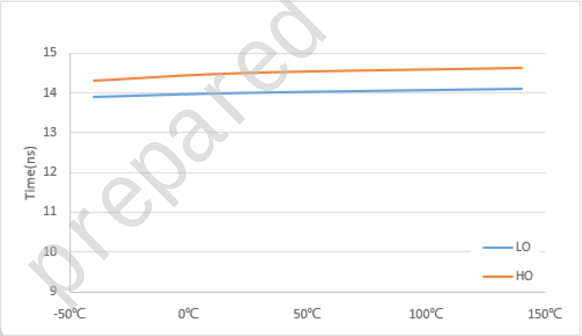


Figure 20. Turn On Propagation Delay vs Temperature

Temp=25℃,C_{L_HO}= C_{L_LO}=0nF

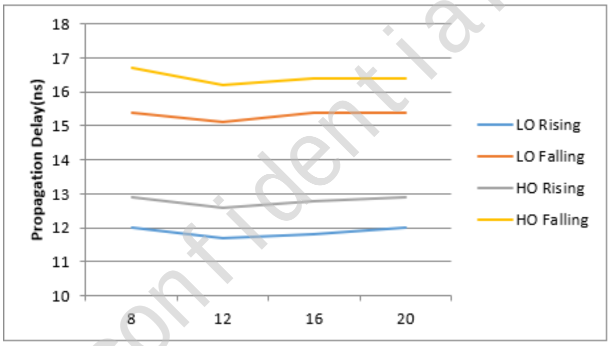


Figure 21. Propagation Delay vs Supply Voltage

VDD=12V,C_{L_HO}= C_{L_LO}=1nF

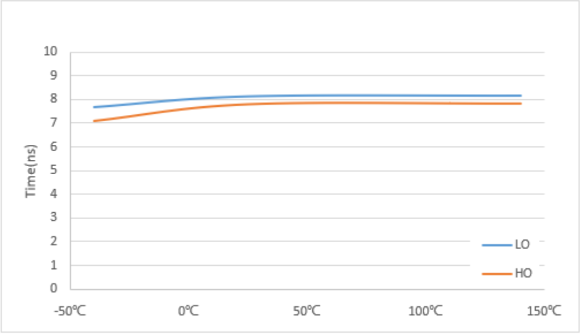


Figure 22. Rising Time vs Temperature

VDD=12V,C_{L_HO}= C_{L_LO}=1nF

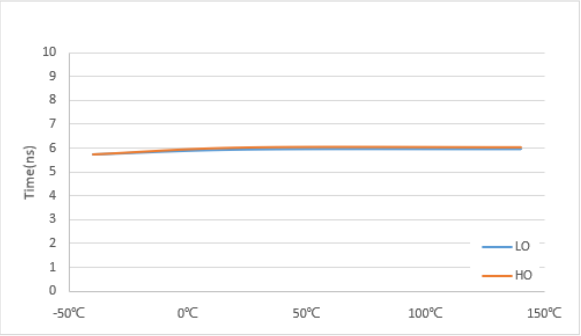


Figure 23. Falling Time vs Temperature

VDD=12V

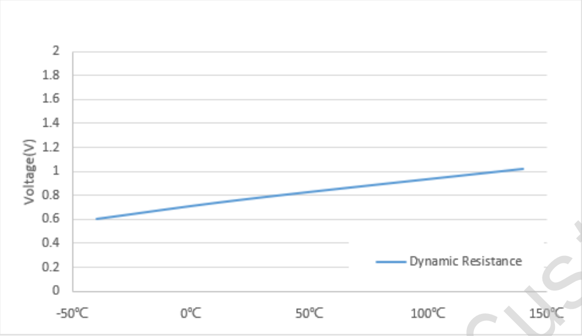


Figure 24. Dynamic resistance vs Temperature

7. Detailed Descriptions

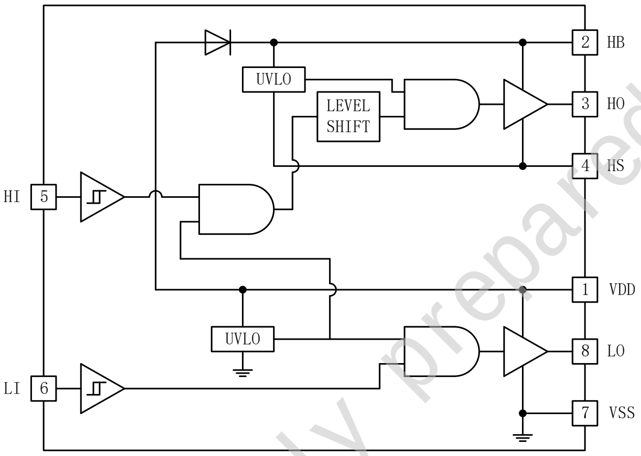
7.1 Overview

MD18211A is high-side and low-side driver which is designed to drive N-Channel MOSFETs in a half-bridge, full-bridge, synchronous-buck, synchronous-boost, push-pull, two-switch forward and active clamp forward converters.

The high-side and low-side each have independent inputs which allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the MD18211A.

MD18211ATDAC: The net weight of a single capsule is 42.74mg.

7.2 Functional Block Diagram



7.3 Functional Modes

MD18211A operates in normal mode and UVLO mode. In the normal mode, the output state is dependent on states of the input pins. See as below:

HI PIN	LI PIN	HO PIN	LO PIN
L	L	L	L
H	L	H	L
L	H	L	H
H	H	H	H

Notes:

(1) HO is measured with respect to HS

(2) LO is measured with respect to VSS

7.4 Input Stages

The input stages provide the interface to the PWM out signals and both input pins are independent. The input is compatible on TTL input-threshold logic that is independent of the VDD supply voltage. There is a pulldown resistance between LI(HI) and VSS (ground), and the resistance is used to make sure 'Low' logic when the VDD start to rise.

With typical high threshold and typical low threshold, MD18211A is conveniently controlled by 3.3V and 5V PWM controller devices.

7.5 Output Stages

The output stages are the interface to the power MOSFETs. Low resistance and high peak current capability of both outputs allow for efficient switching of the power MOSFETs. The low side output stage is referenced from VDD to VSS and the high side is referenced from HB to HS.

MD18211A provides excellent output negative voltage handling capability, thanks to its high peak current driving capability and 2kV HBM and 2kV CDM ESD performance.

7.6 Boot Diode

The boot diode is connected VDD pin to HB pin and used to charge the boot capacitor connected HB pin to HS pin. When HS pin transitions to ground, the current of VDD charge the boot capacitor until HS rising. The boot diode provides fast recovery time, low equivalent resistance and voltage rating to allow for reliable operation.

7.7 Undervoltage Lockout (UVLO)

The supplies for the high-side (HB to HS) and low-side (VDD to VSS) are monitored. When the voltage of VDD is below the specified threshold, the VDD UVLO disables low-side driver and send the signal by level shift to disable high-side driver. When the voltage of HB to HS is below the specified threshold, the HB UVLO disables only the high-side driver.

7.8 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

8. Application And Implementation

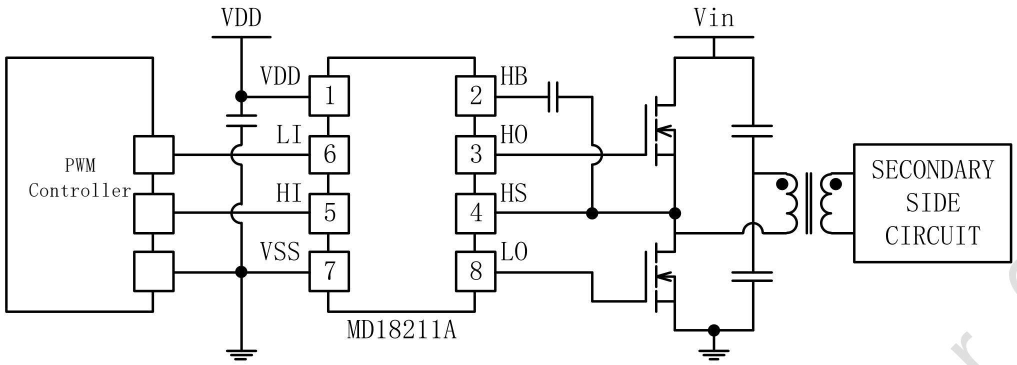


Figure 25. MD18211A Typical Application: Half Bridge

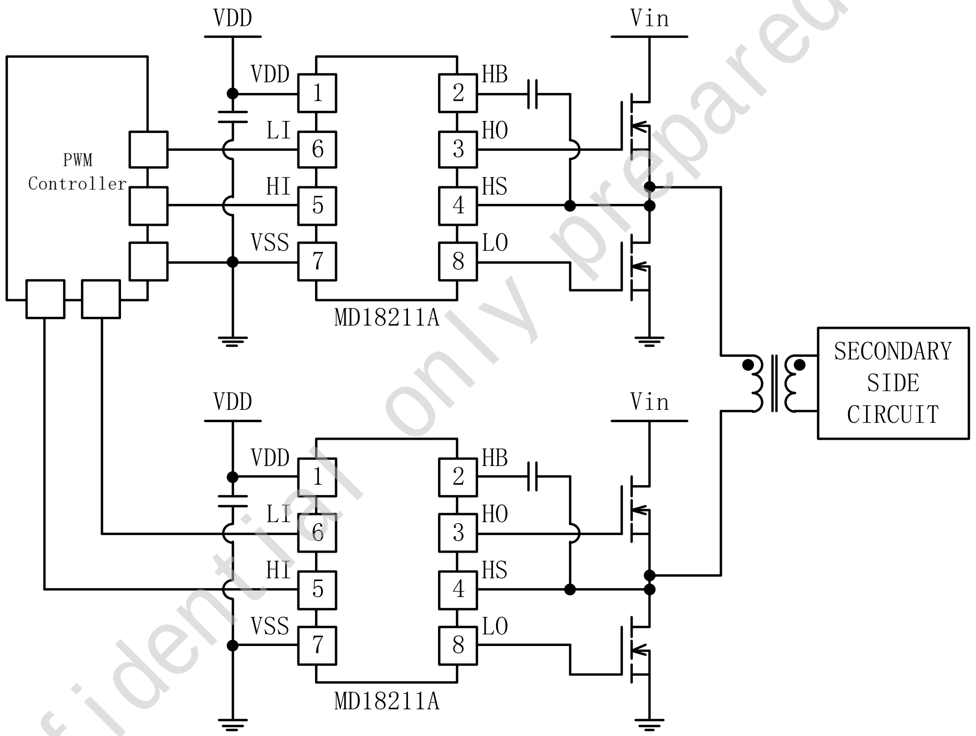


Figure 26. MD18211A Typical Application: Full Bridge

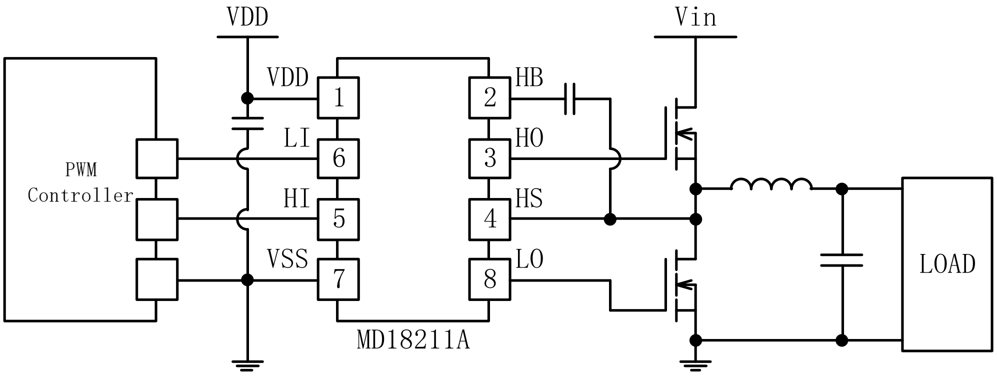


Figure 27. MD18211A Typical Application: Buck

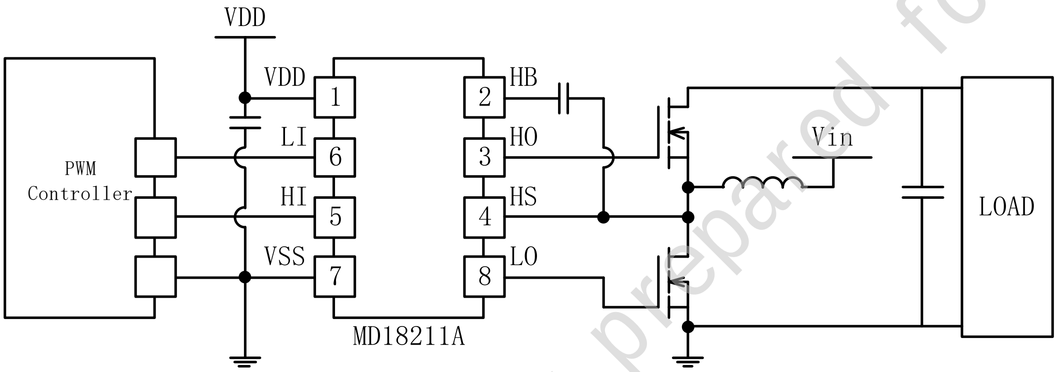


Figure 28. MD18211A Typical Application: Boost

9. Design Procedure

9.1 Input Threshold Type

The MD18211A has an input maximum voltage range from -10V to 20V and can be directly interfaced to gate drive transformers. The MD18211A threshold voltage levels are independent of the VDD supply voltage, which allows compatibility with both logic-level input signals from MCU, DSP as well as analog controllers.

For system application, if there is long trace from PWM controller to driver, it is suggested that adding a RC filter close to HI pin and LI pin.

9.2 Supply Voltage

The supply voltage to be applied to the VDD pin of the driver should never exceed the absolute maximum rating. Higher voltage can reduce the conduction loss of MOSFET, and increase the switching loss.

The choice of HB-HS capacitor and VDD-VSS capacitor should be dependent on the switching frequency and C_{gs} of MOSFET. Use 100nF(50V) as HB-HS capacitor and 10uF(50V) paralleled with 100nF(50V) as VDD-VSS capacitor in the general. The function of paralleled capacitor is decoupling.

9.3 Peak Source and Sink Currents

The switching speed of the MOSFET during turning-on and turning-off should be as fast as possible in order to minimize switching power losses. The gate driver must be able to provide the required peak current for achieving the targeted switching speeds with the targeted power MOSFET.

For system application, adding a resistance (such as 1Ω or 2.2Ω) between gate of MOSFET and LO/HO can control the switching speed of the MOSFET. The faster turning-on speed, the higher the stress of Drain-Source of MOSFET, and the lower switching loss.

9.4 Propagation Delay

The propagation delay from the gate driver is dependent on the switching frequency and Cgs of MOSFET. The MD18211A ensures very little pulse distortion and allows operation at very high-frequency.

When using MD18211A as driver in Boost, Buck, synchronous rectification, PWM controller need to reserve enough deadtime between HI and LI.

9.5 Power Dissipation

Power dissipation of MD18211A has two portions as below

$P_{DISS} = P_{DC} + P_{SW}$

The DC portion of the power dissipation is

$P_{DC} = IQ * VDD$

Where IQ is the quiescent current for MD18211A. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, level shift circuits, UVLO circuit, and also any current associated with switching of internal devices when the driver output changes state.

The switching portion of the power dissipation include:

1) switching frequency
2) QG of the MOSFET
3) Supply voltage VDD

$PSW = QG * VDD * f_{SW}$

10. Layout

10.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules must be followed.

(1) Locate the driver close to the MOSFETs.
(2) Locate the VDD-VSS and HB-HS capacitors close to the driver.
(3) Connect the VSS pin to thermal pad and use the thermal pad as GND. The GND trace from MD18211A does directly to the source of the low-side MOSFET, but not be in the high current path of MOSFET source current.
(4) Use the same rules for HS as for GND for the high-side MOSFET.
(5) For system using multiple drivers, the decoupling capacitors need to be located at VDD-VSS for each driver.
(6) Avoid placing VDD, LI, HI trace close to LO, HS and HO signals or any other high dV/dT traces that can induce significant noise into the high impedance leads.
(7) Use wide trace for LO and HO to decrease the influence of switching ringing made by parasitic inductance.
(8) If the driver outputs or SW node must be routed from one layer to another, use at least two vias.
(9) For GND, the number of vias must be a consideration of the thermal pad requirements as well as minimizing parasitic inductance.

10.2 Layout Example

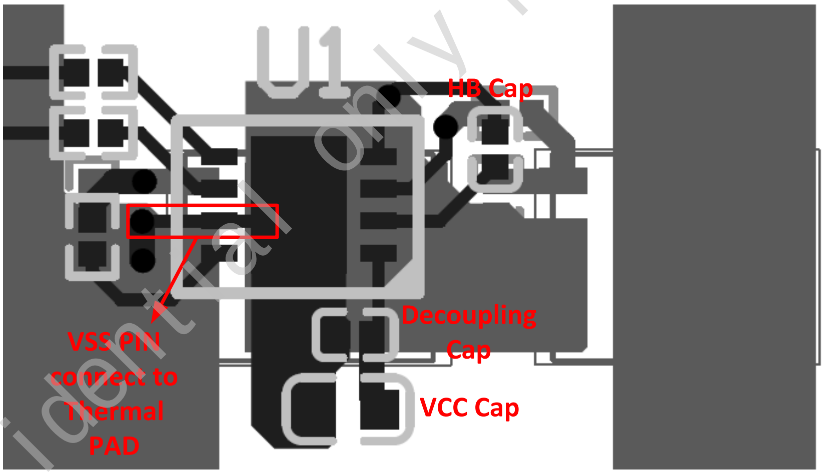


Figure 29. Layout Example

11. Tape and Reel Information

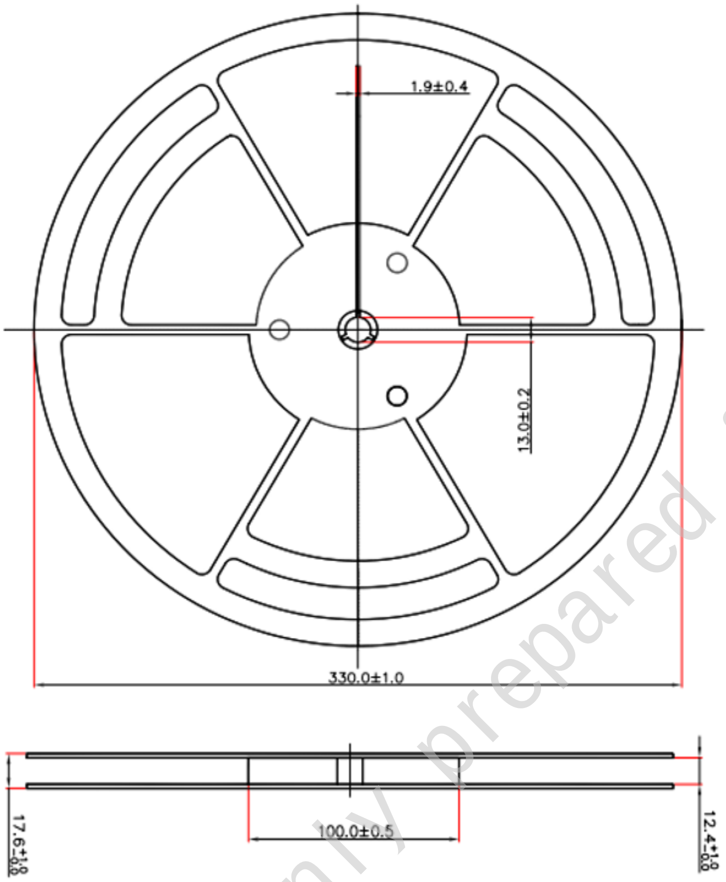


Figure 30. Reel Dimensions

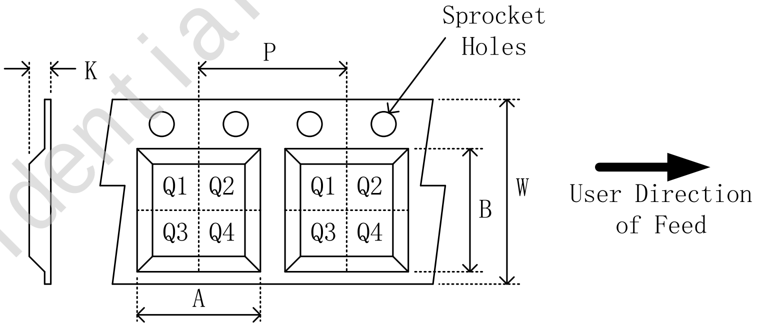
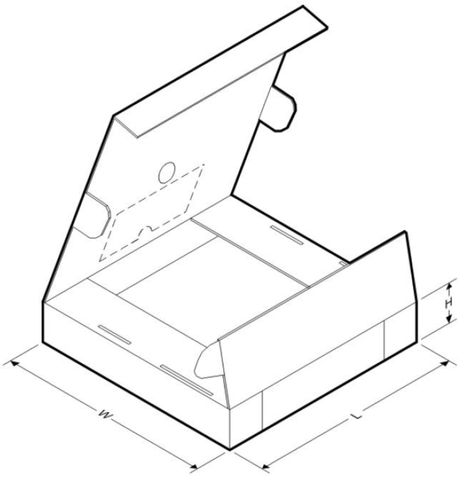


Figure 31. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant
MD18211ATDAC	DFN 4X4	8	5000	4.3±0.1	4.3±0.1	1.1±0.1	8.0±0.1	4±0.1	12.0±0.3	Q1
MD18211ATAD	ESOP	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8±0.1	4±0.1	12±0.1	Q1
MD18211ATDD	DFN 4X4	10	5000	4.3±0.1	4.3±0.1	1.1±0.1	8.0±0.1	4±0.1	12.0±0.3	Q1

12. Tape and Reel Box Dimensions




PART NO.: MD18211ATDAC
RANGE:
PACKAGE: DFNQFN 4X4X0.75 8
QUANTITY: 5000PCS
DATE CODE: XXXXXXXXX
LOT NO.: XXXXXXX
DATE: XXXX/XX/XX
茂睿芯 MERAKI INTEGRATED
HF GP Pb
WF: C01/W01
AT: C02/A01

(please refer to MRX-DM-SCM-04 for detailed rules)

Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MD18211ATDAC	DFN 4X4	8	5000	360	360	65
MD18211ATAD	ESOP	8	8000	360	360	65
MD18211ATDD	DFN 4X4	10	5000	360	360	65

Figure 32. Box Dimensions

13. Mechanical Data and Land Pattern Data

13.1 DFN 4X4-8

13.1.1 Mechanical Data

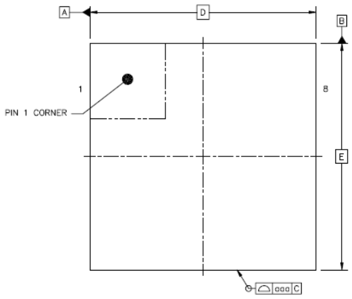


Figure 33. DFN 4X4-8 Top View

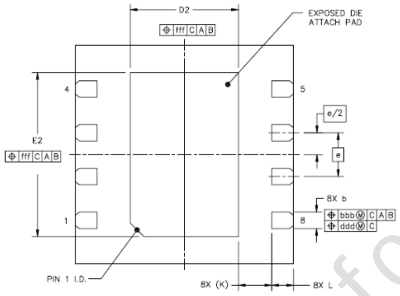


Figure 34. DFN 4X4-8 Bottom View

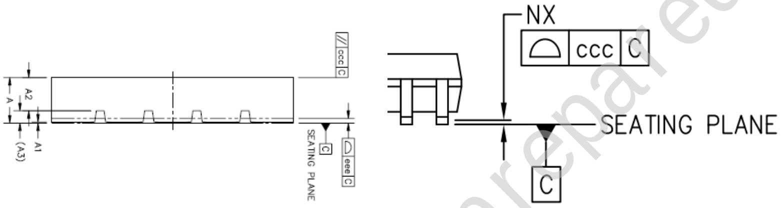


Figure 35. DFN 4X4-8 Side and Coplanarity View

Symbol	Min (mm)	Nom (mm)	Max (mm)
A	0.70	0.75	0.80
A1	-	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
B	0.25	0.3	0.35
D	4 BSC		
E	4 BSC		
E	0.8 BSC		
D2	1.88	1.98	2.08
E2	2.9	3	3.1
L	0.30	0.40	0.50
K	0.61 REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
ddd	0.05		
fff	0.1		
Coplanarity(ccc) ≤ 0.10mm			

13.1.2 Land Pattern Data

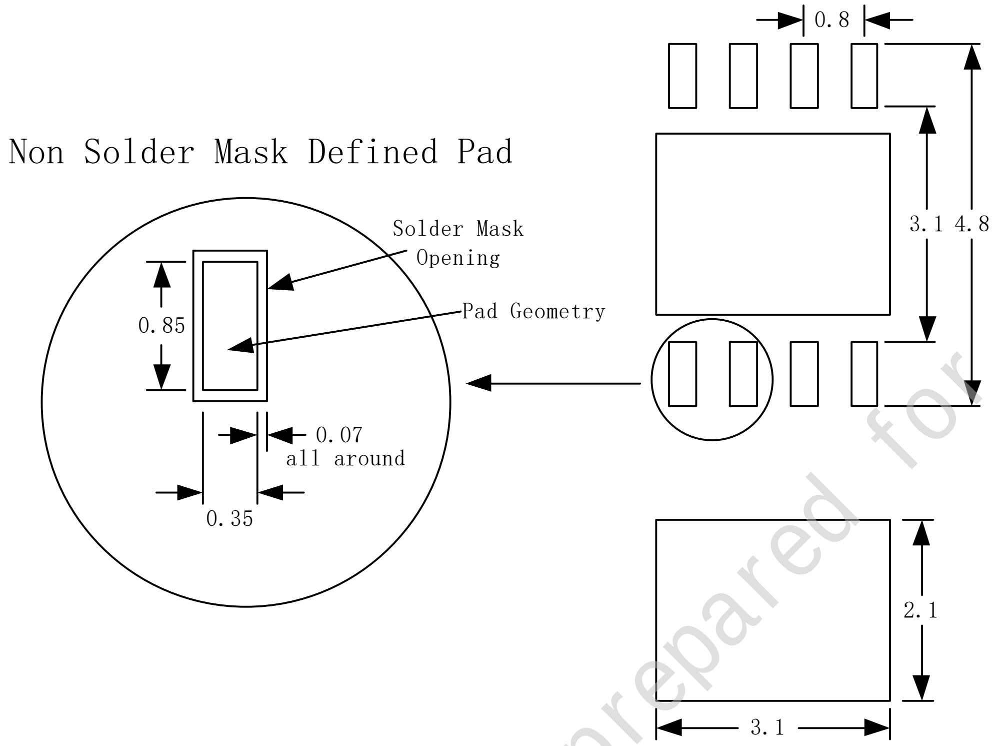


Figure 36. DFN-8 4X4 Land Pattern Data

13.2 ESOP-8

13.2.1 Mechanical Data

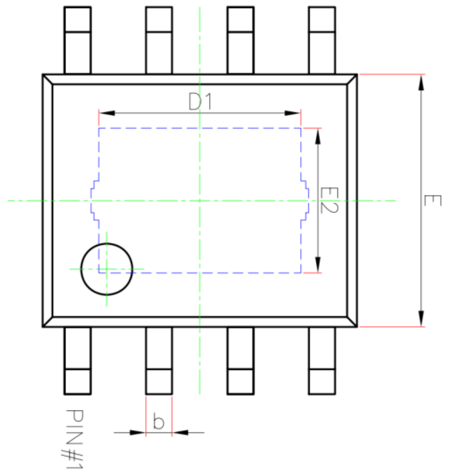


Figure 37. ESOP-8 Top View

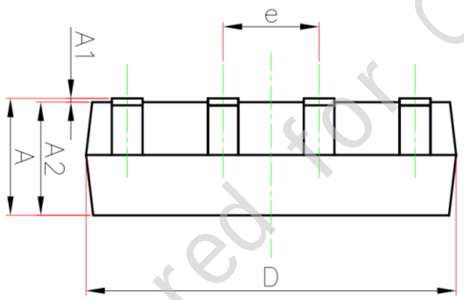


Figure 38. ESOP-8 Side View

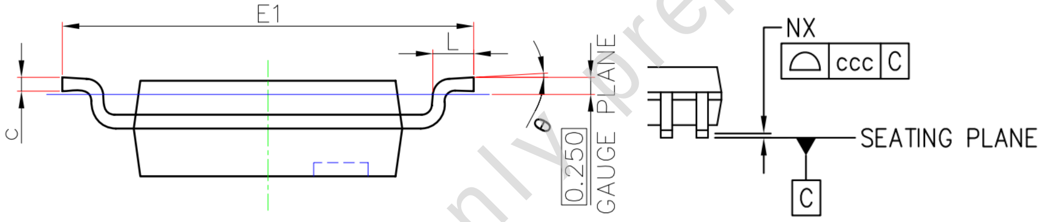


Figure 39. ESOP-8 Side and Coplanarity View

Symbol	Millimeter		
	Min	Nom	Max
A	1.30	1.50	1.70
A1	0.00	-	0.10
A2	1.35	1.45	1.55
b	0.33	-	0.51
c	0.17	-	0.25
D	4.70	4.90	5.10
D1	3.05	3.90	3.25
E	3.80	6.00	4.00
E1	5.80	3.15	6.20
E2	2.16	2.26	2.36
e	1.27(BSC)		
L	0.40	-	1.27
θ	0°	-	8°
Coplanarity(ccc) ≤ 0.10mm			

13.2.2 Land Pattern Data

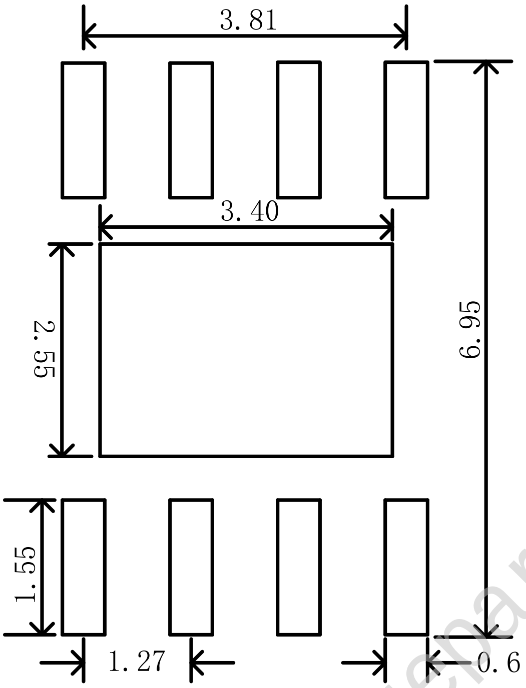


Figure 40. ESOP-8 Land Pattern Data

13.3 DFN 4X4-10

13.3.1 Mechanical Data

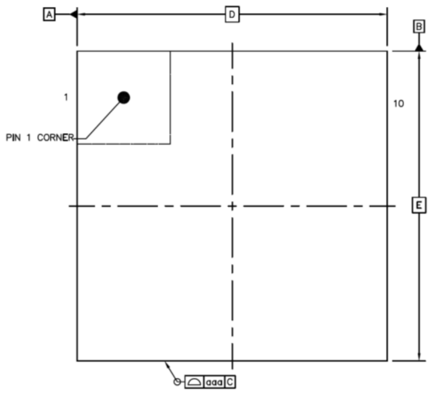


Figure 41. DFN 4X4-10 Top View

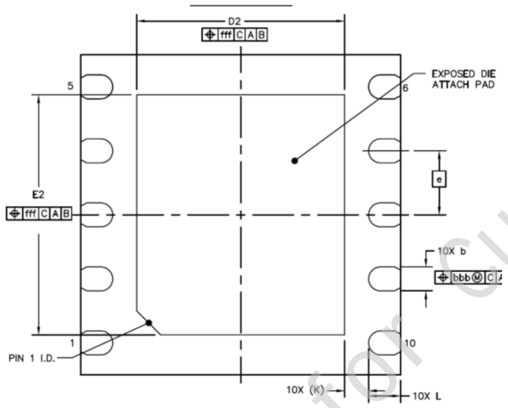


Figure 42. DFN 4X4-10 Bottom View

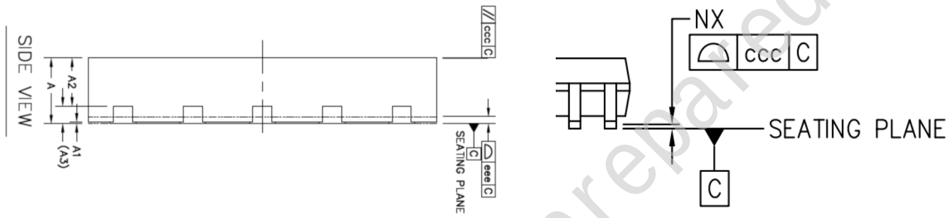


Figure 43. DFN 4X4-10 Side and Coplanarity View

Symbol	Min (mm)	Nom (mm)	Max (mm)
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	---	0.55	---
A3	0.203 REF		
b	0.25	0.3	0.35
D	4 BSC		
E	4 BSC		
e	0.8 BSC		
D2	2.5	2.6	2.7
E2	2.9	3	3.1
L	0.3	0.4	0.5
K	0.3 REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
fff	0.1		
Coplanarity(ccc) ≤ 0.10mm			

13.3.2 Land Pattern Data

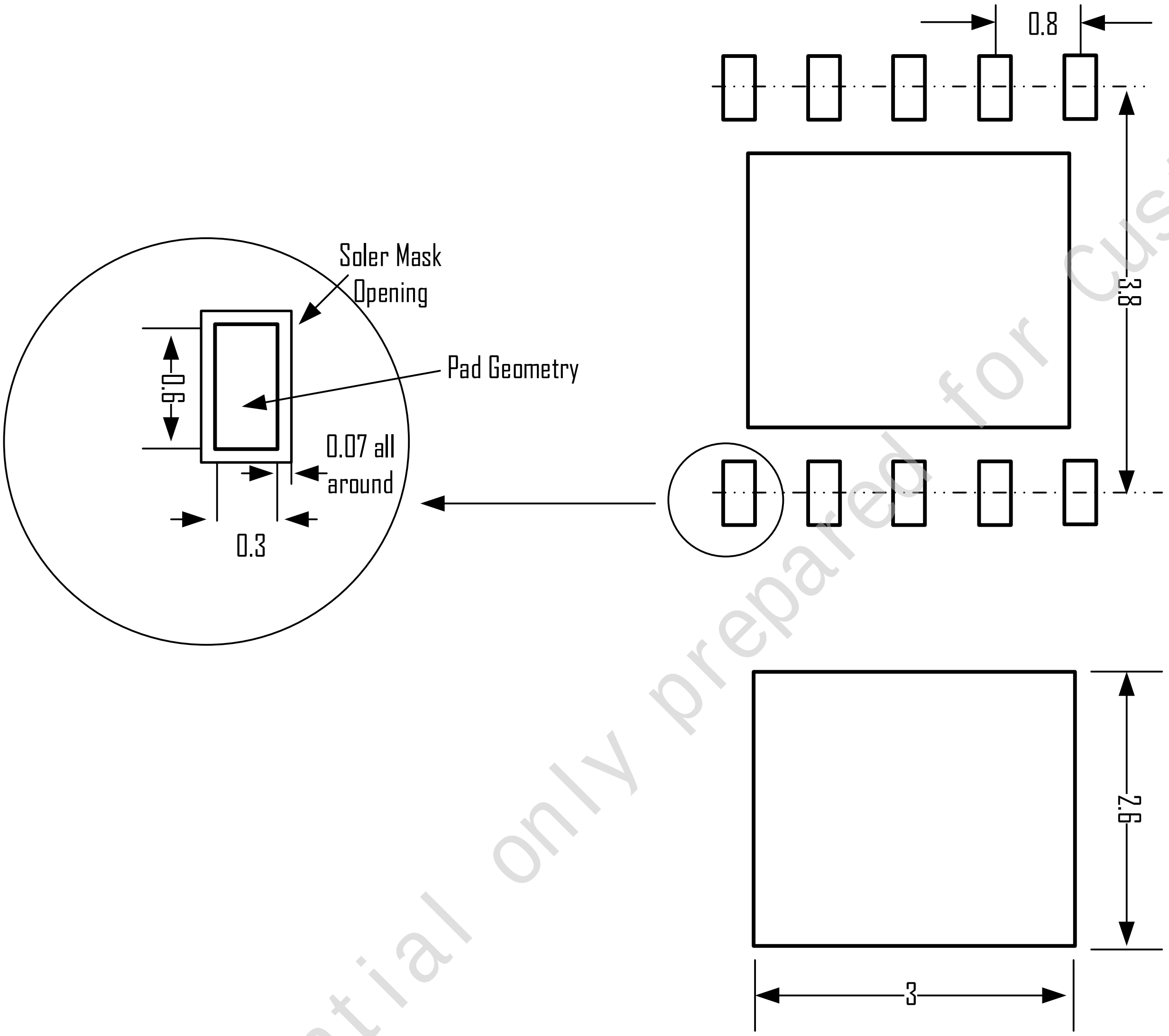


Figure 44. DFN 4X4-10 Land Pattern Data